Cache-Timing Attack Against HQC

Chitchanok Chuengsatiansup

The University of Melbourne, Australia

About Me

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2023 **Senior Lecturer:** The University of Melbourne, Australia

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2017 **Post-doc:** Ecole Normale Supérieure de Lyon, France

2013 **PhD Student:** Technische Universiteit Eindhoven, The Netherlands

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2011 **Master's Student:** The University of Tokyo, Japan

2010 **Research Student:** The University of Tokyo, Japan

2006 **Bachelor's Student:** Chulalongkorn University, Thailand

Efficient and Secure Cryptosystems

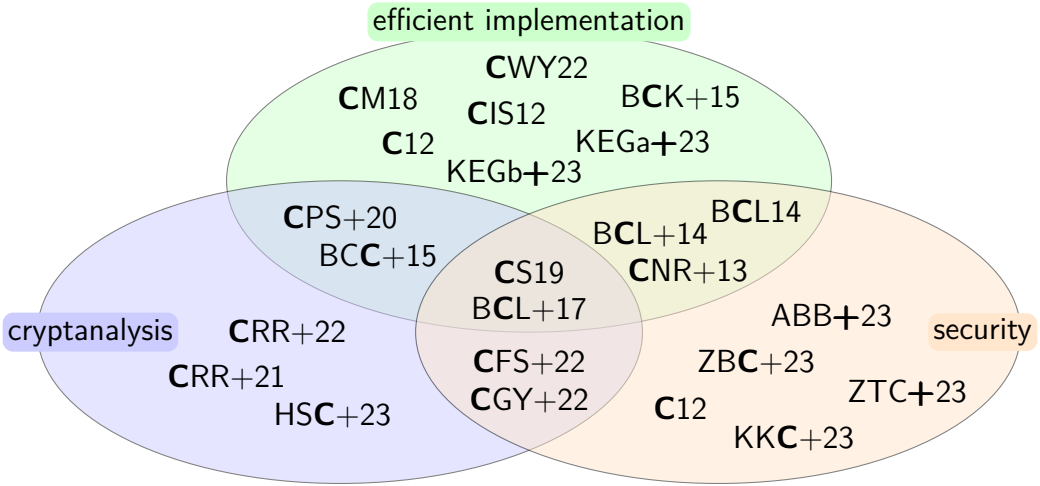
Efficient and Secure Cryptosystems

efficient implementation

cryptanalysis

security

Efficient and Secure Cryptosystems



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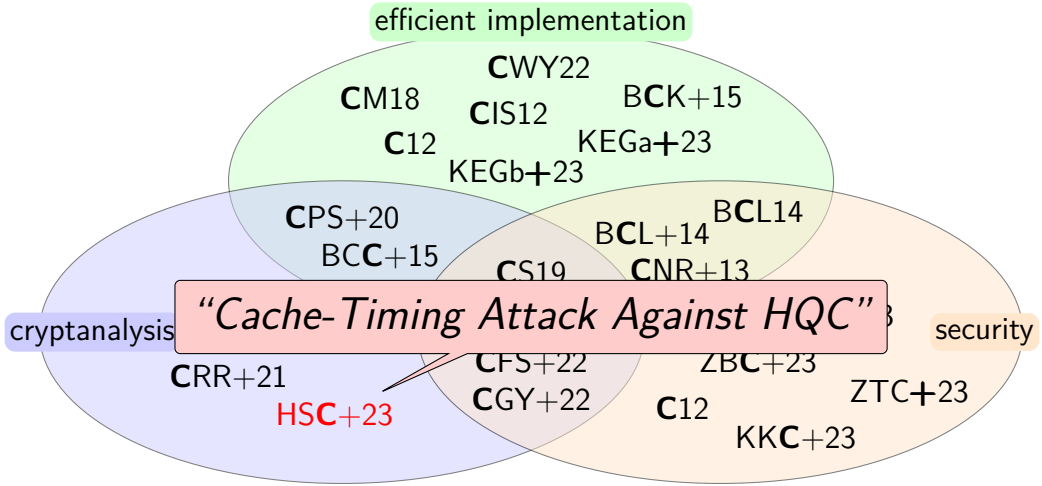

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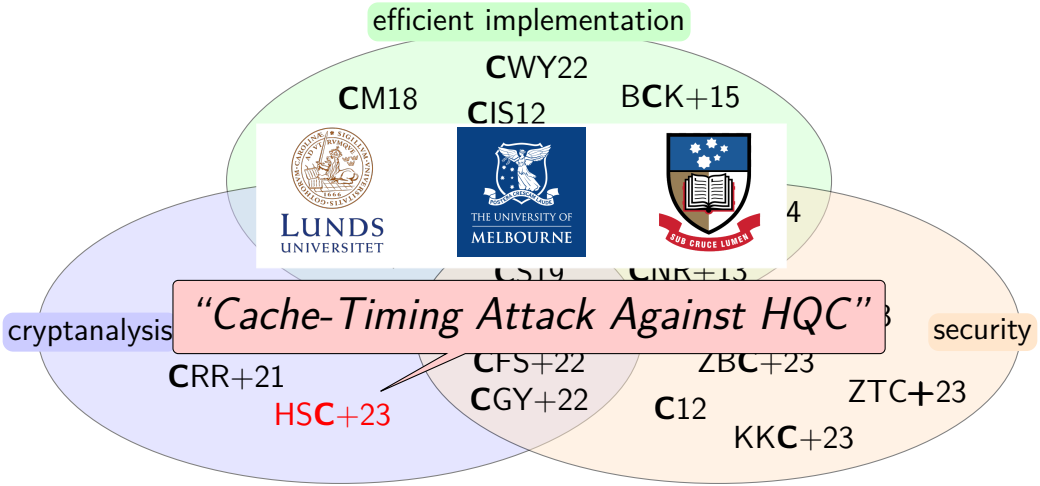

Joint work with Senyang Huang, Rui Qi Sim, Qian Guo, and Thomas Johansson

Optimization Strategy

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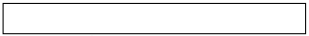
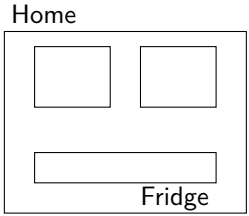
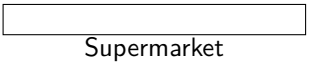


Supermarket

Optimization Strategy





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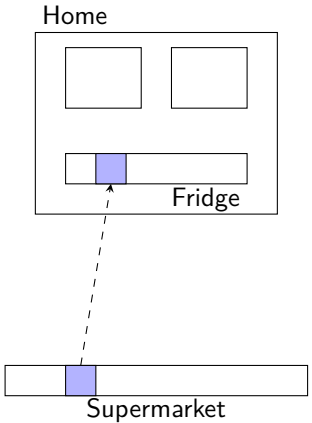

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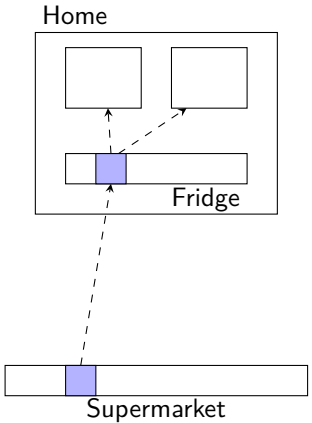
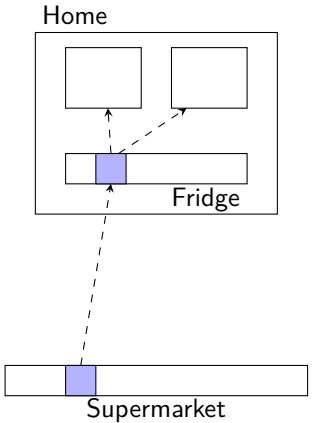


Optimization Strategy

- Exchanging products at a supermarket shortens customers' time



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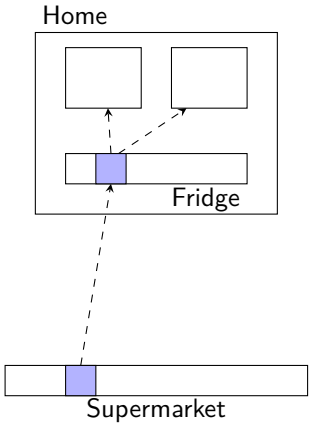
- Exchanging products at a supermarket shortens customers' time
- Storing food in a fridge to avoid frequent visits to a supermarket



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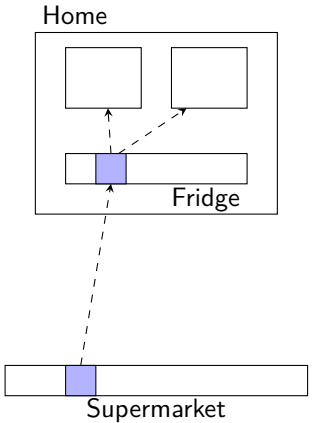
- Storing food in a fridge to avoid frequent visits to a supermarket
- Observing shopping patterns can deduce food menus or recipes



Speeding Up Performance

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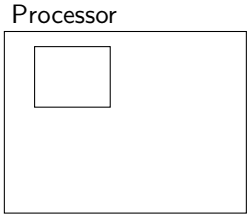

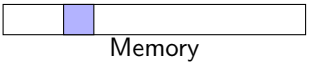

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  - spatial: divide memory into lines
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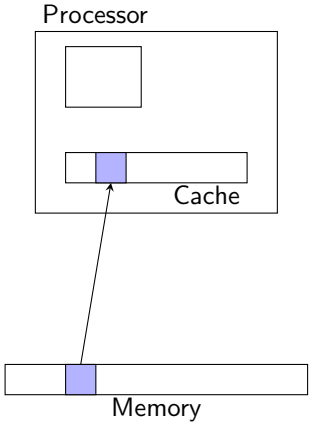

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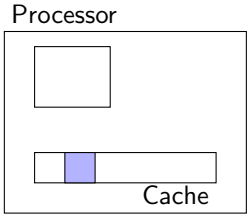

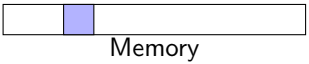

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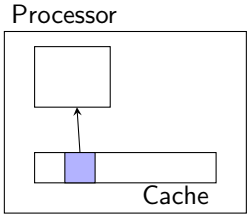

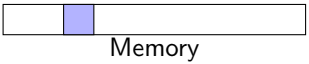

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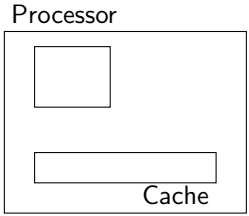

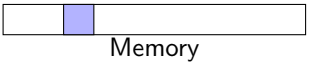

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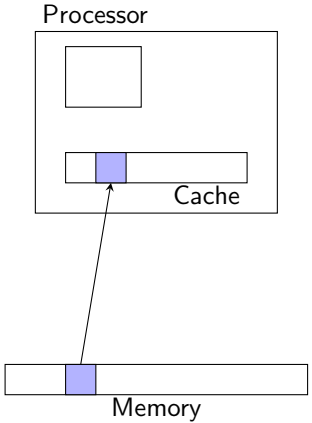

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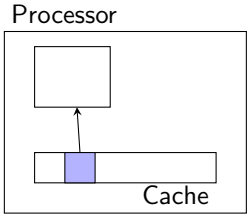

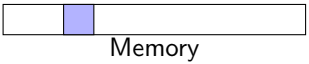

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- Check if data is in cache
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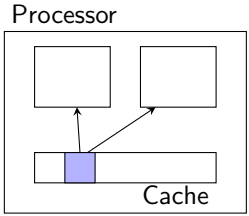
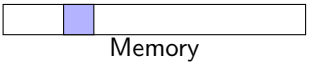
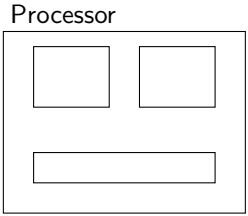
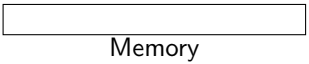
- Share cache
  - improve performance of multi-core processors





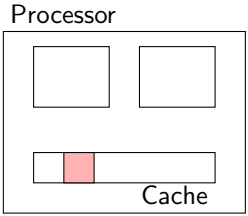
Maintaining Consistency

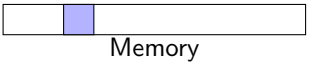




Maintaining Consistency

- Memory and cache can be inconsistent
  - rare but possible





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- Memory and cache can be inconsistent
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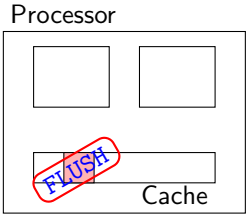
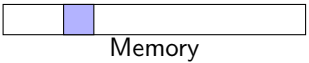
- Solution: flush cache contents
  - ensure next load to serve from memory





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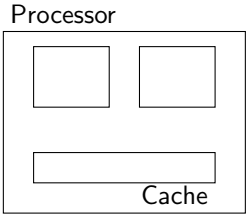

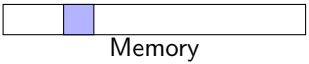

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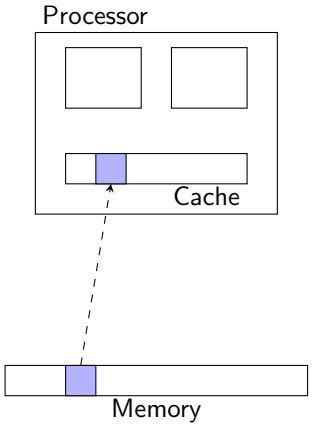

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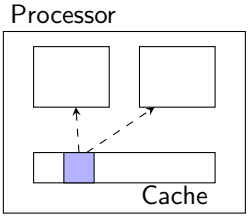
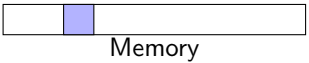
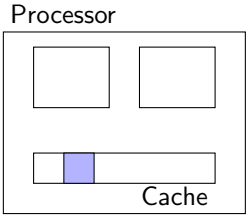
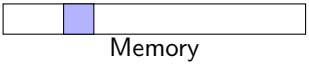




Flush + Reload [GBK11, YF14]





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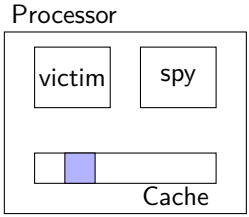

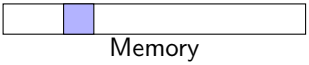

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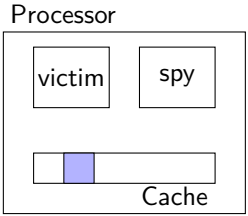

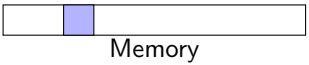

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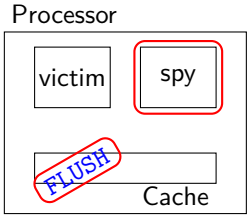

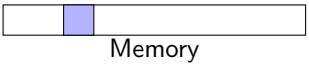

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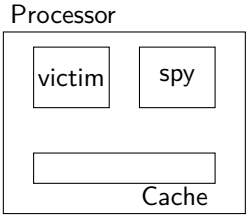

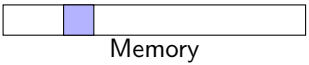

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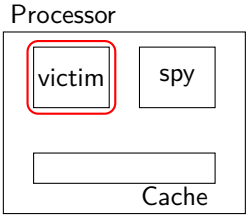

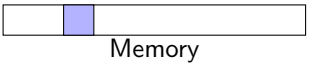

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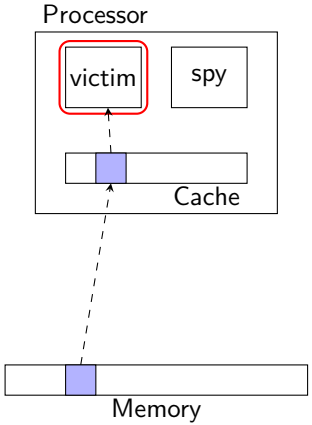

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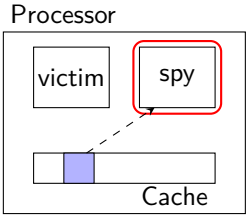

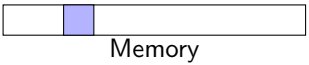

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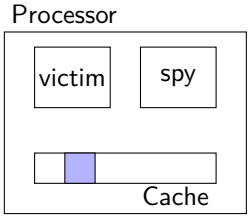
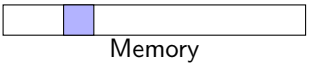
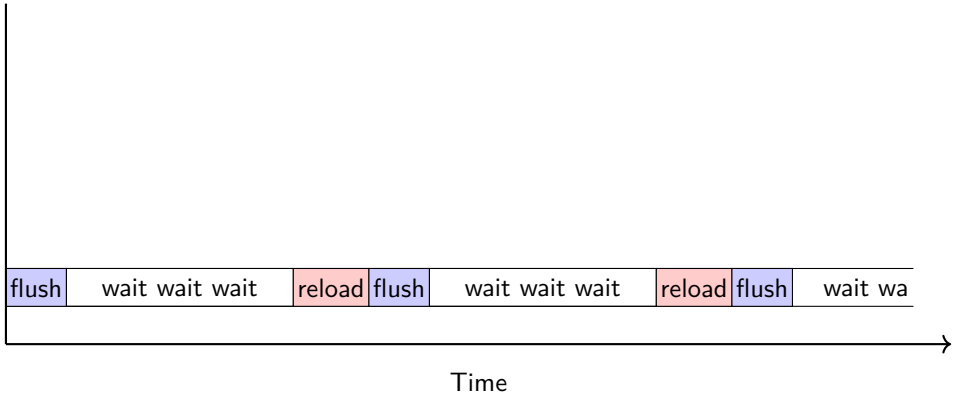
- **Flush** memory line
- Wait (victim executes)
- Measure time to **Reload** line
  - slow → no victim access
  - fast → victim accessed
- (Repeat)





Flush + Reload: in action



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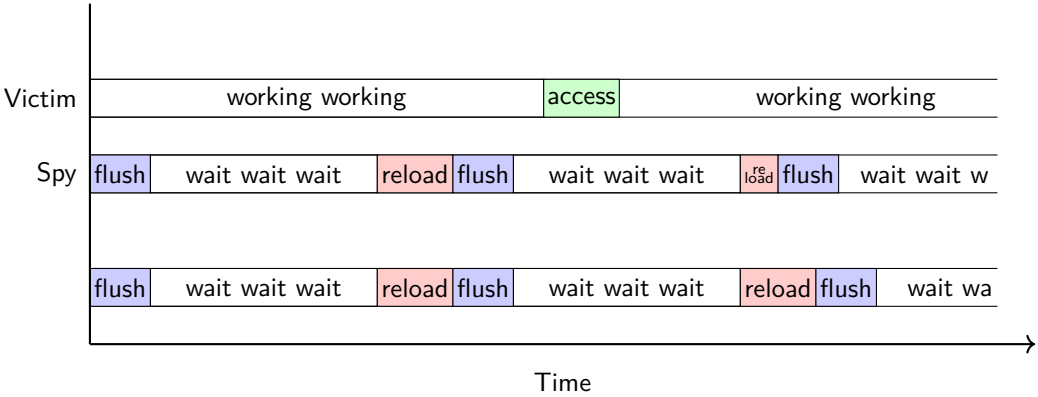

Flush + Reload: pros & cons

+ Simple
+ Very fews false positive
+ Resolution of memory line

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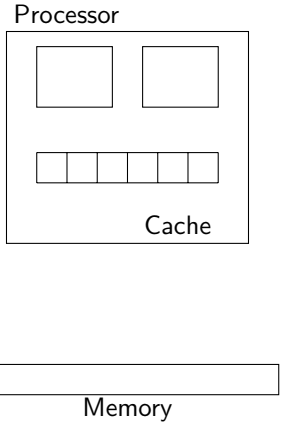
+ Very fews false positive
+ Resolution of memory line

- Only work with shared memory
- Require flush instruction

Set Associative Caches



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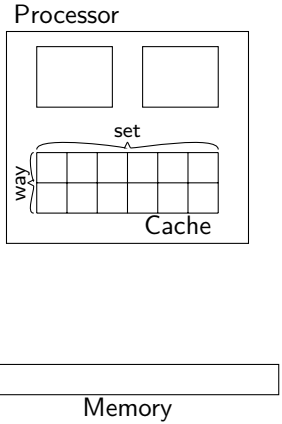
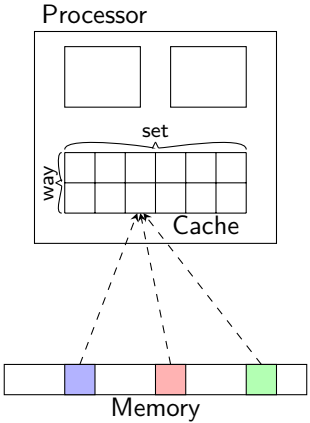


Set Associative Caches

- Memory lines map to cache sets



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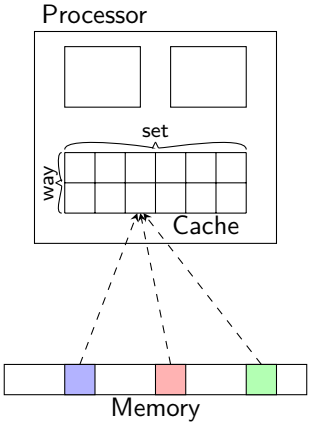

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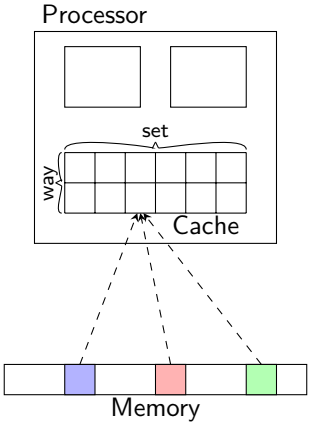

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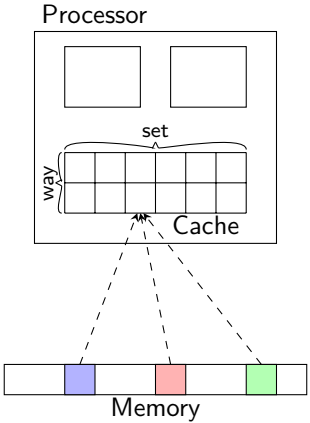

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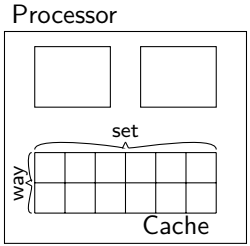

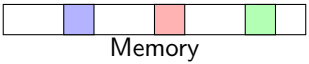

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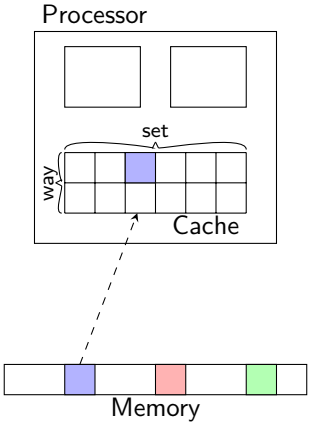

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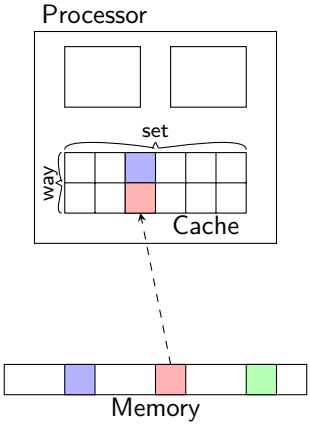

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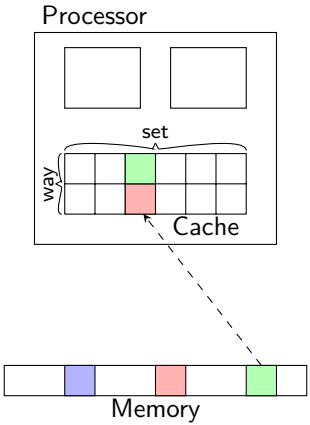

Prime + Probe [OST05, Per05]

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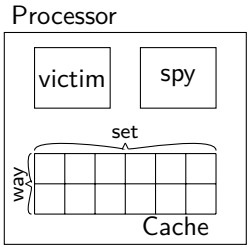

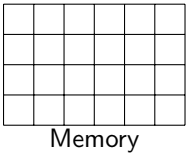

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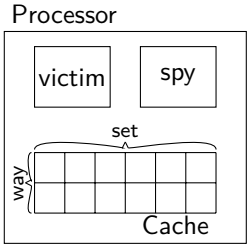

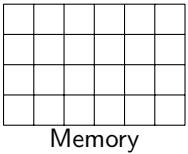

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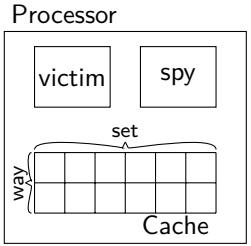

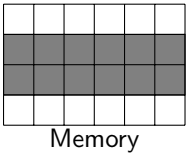

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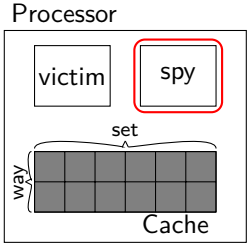

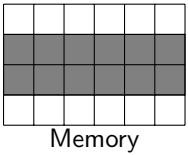

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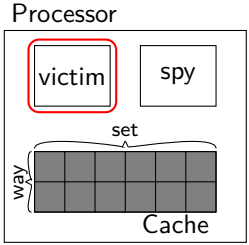

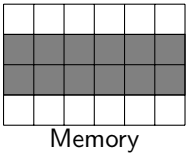

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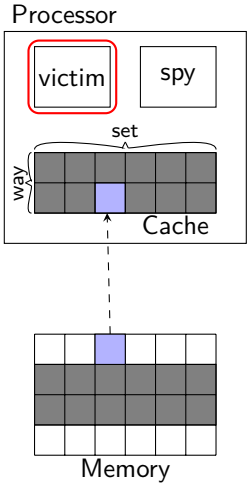

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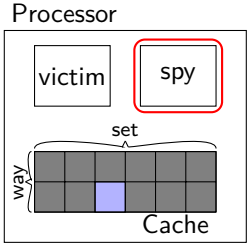

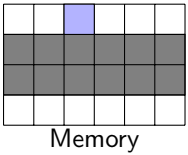

Limitations of Cache-Timing Attacks

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- Provide cache/memory access patterns
  - might not reveal actual secret values

Limitations of Cache-Timing Attacks

- Provide cache/memory access patterns
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- Provide partial information
  - might not reveal the full secret key

HQC

- HQC: Hamming Quasi Cyclic
- 4th-round candidate of the ongoing NIST PQC Standardization
- Code-based post-quantum key encapsulation mechanism (KEM)

HQC's KEM

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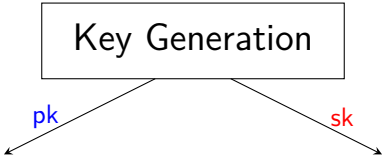
Key Generation

HQC's KEM



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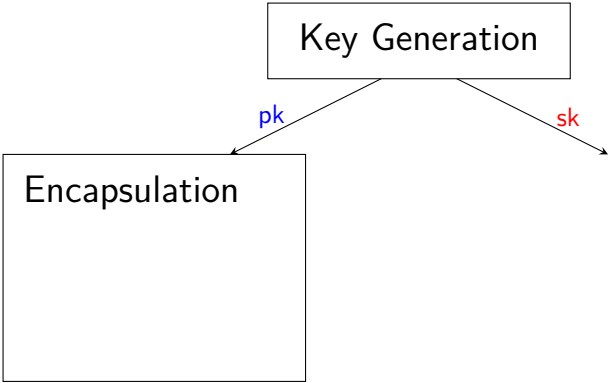

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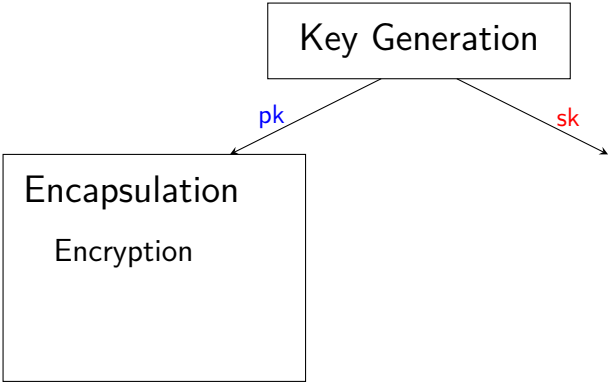

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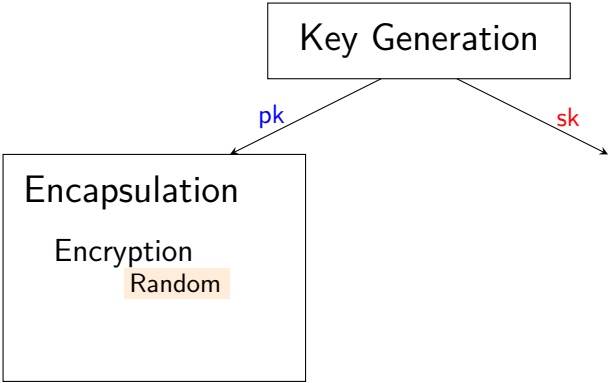

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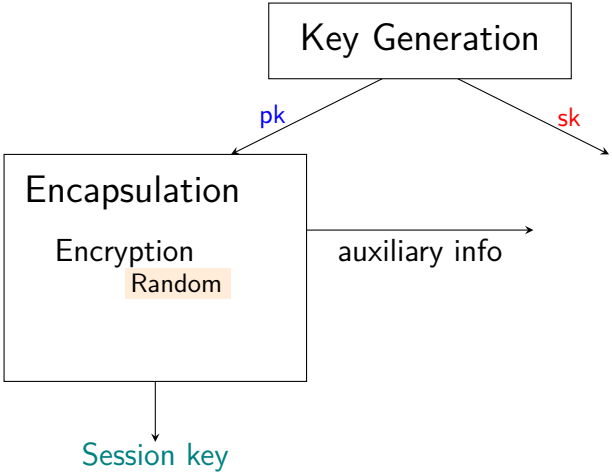
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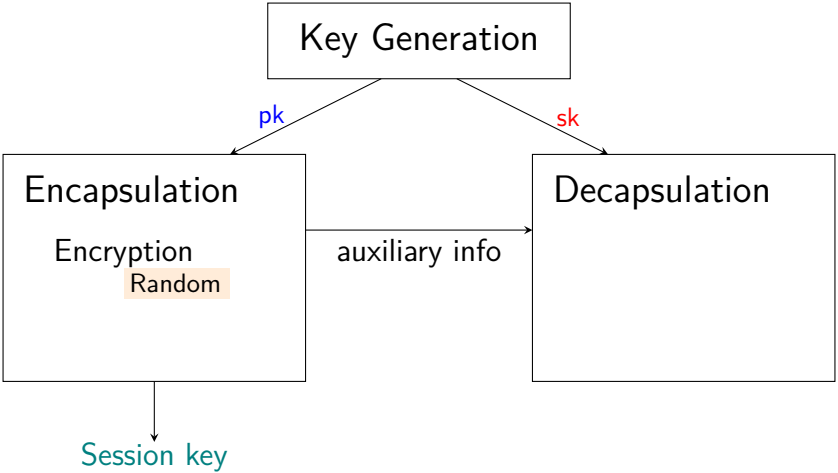
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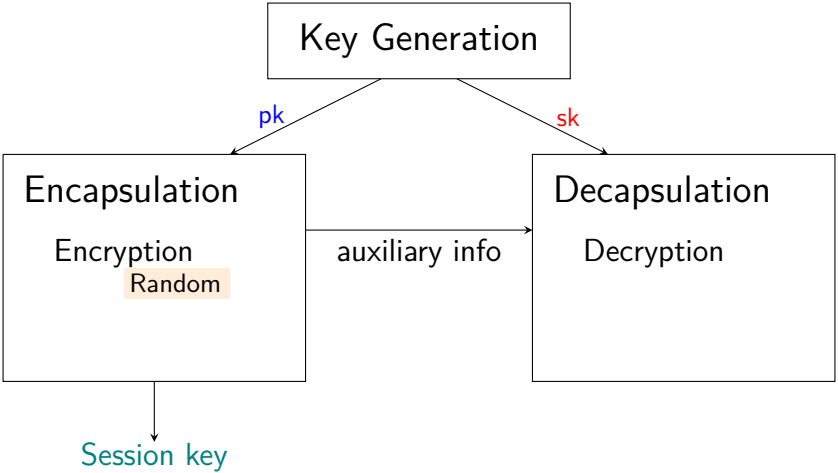
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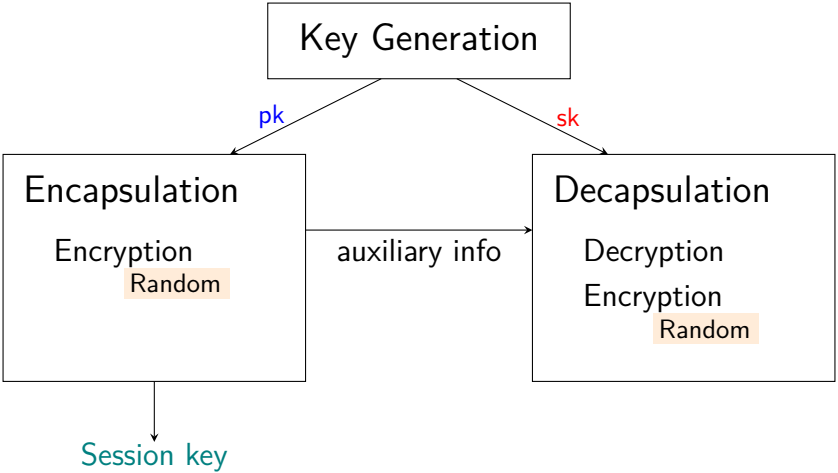
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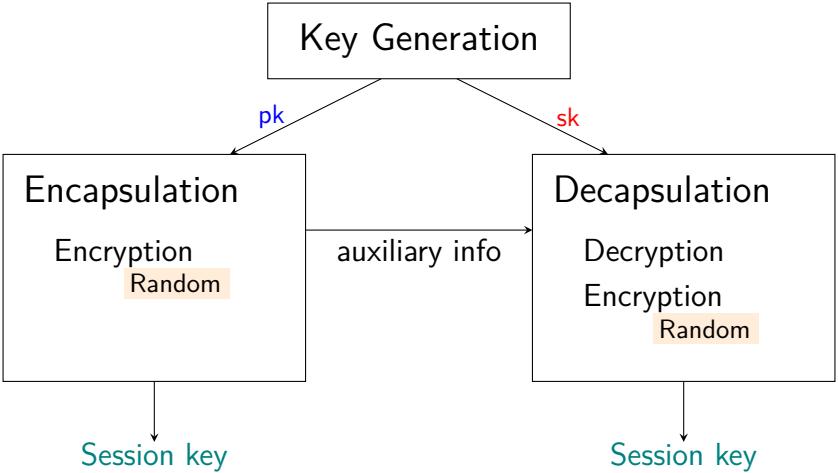
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Randomness

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$c = m + \text{error}$

Randomness

Encryption

$$c = m + \underbrace{\text{error}}_{\text{random+sk}}$$

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$\uparrow$

$m+\text{error}$

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random+sk

Decryption

$c - \text{error'}$

m+error

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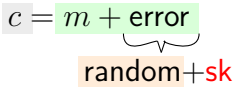

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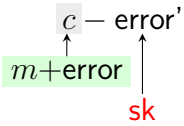

Randomness

Encryption

$c = m + \text{error}$

random+sk

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$m' = c - \text{error'}$

m+error

sk

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$m' = c - \text{error'}$

$m + \text{error}$ ↑ c, sk ↑ error'

$m = m'$ vs $m \neq m'$

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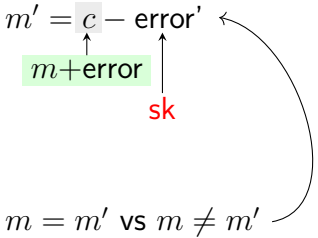

Cache Line Indicator

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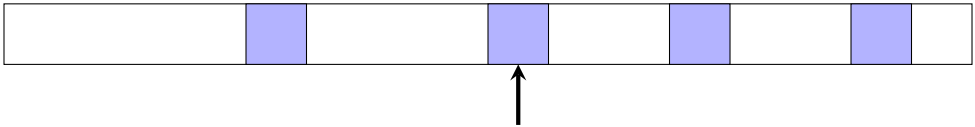

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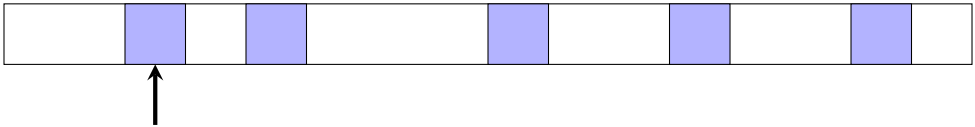

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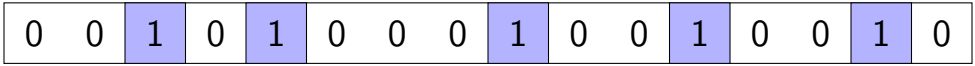

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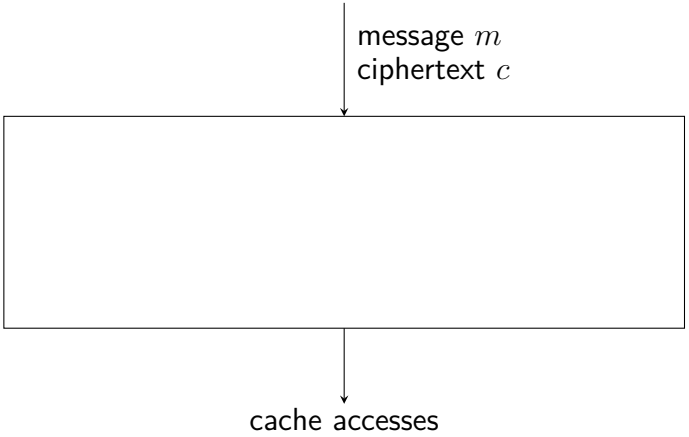

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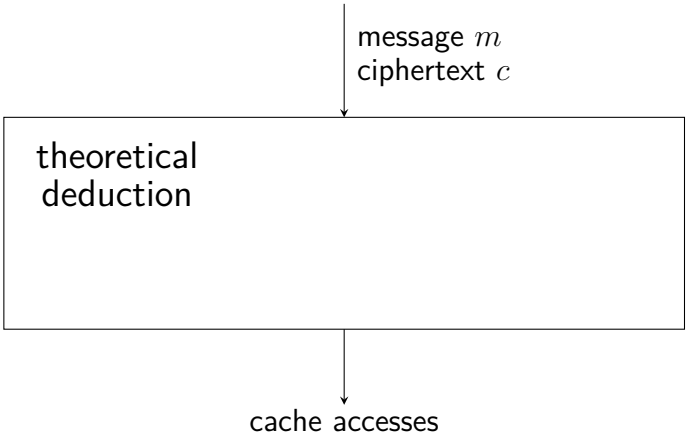
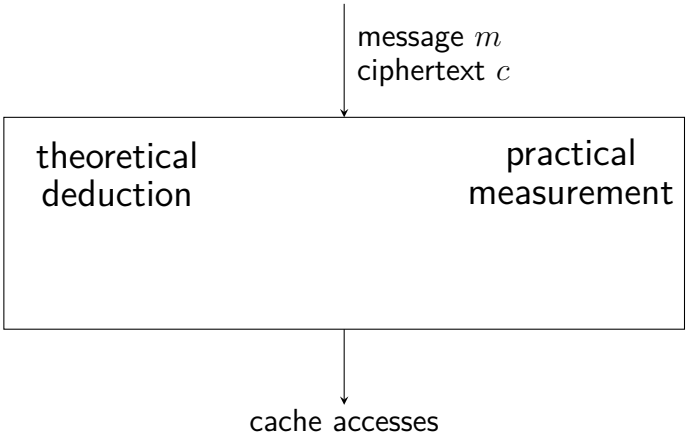


Plaintext-Checking Oracle



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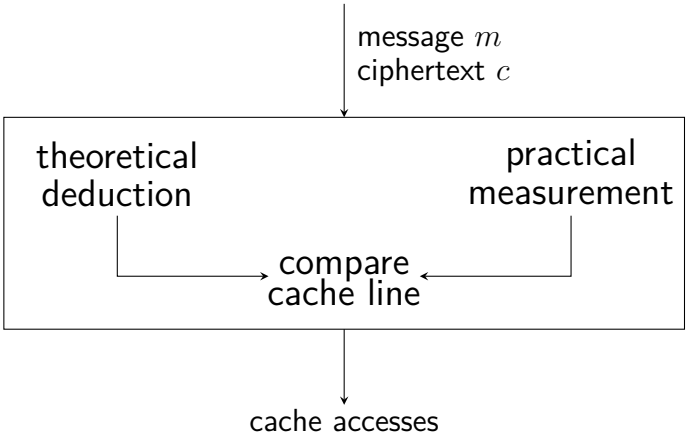

Our Attack

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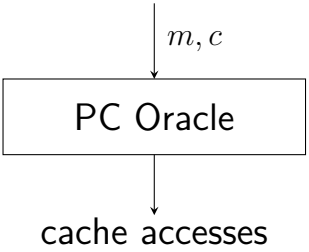

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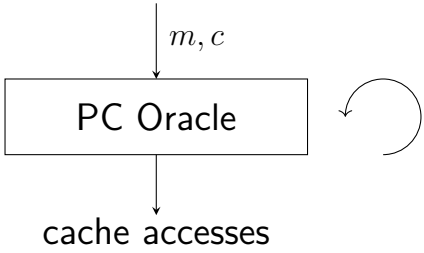

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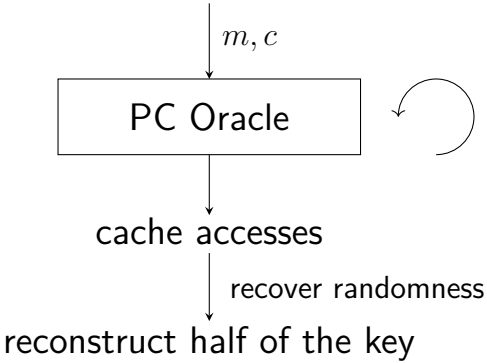
m, c
PC Oracle
cache accesses
recover randomness
reconstruct half of the key

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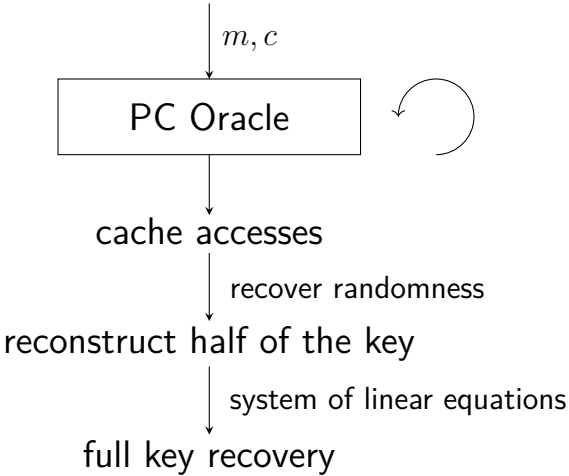
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PC Oracle
cache accesses
recover randomness
reconstruct half of the key
system of linear equations
full key recovery

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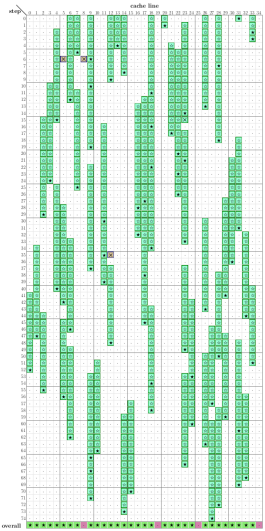

Comparison to ground truth

- ★ true positive
- · true negative
- × false positive
- ☆ speculatively accessed

Simple analysis

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Final classification

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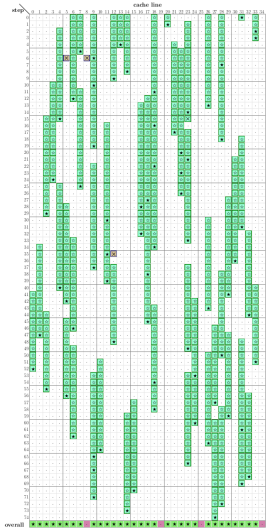

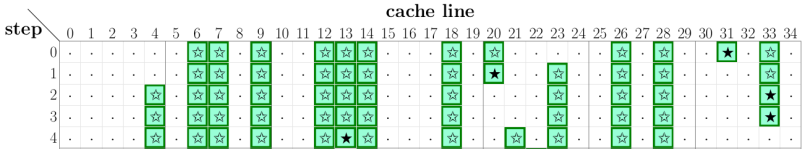

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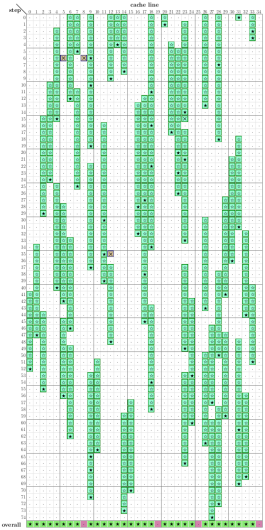

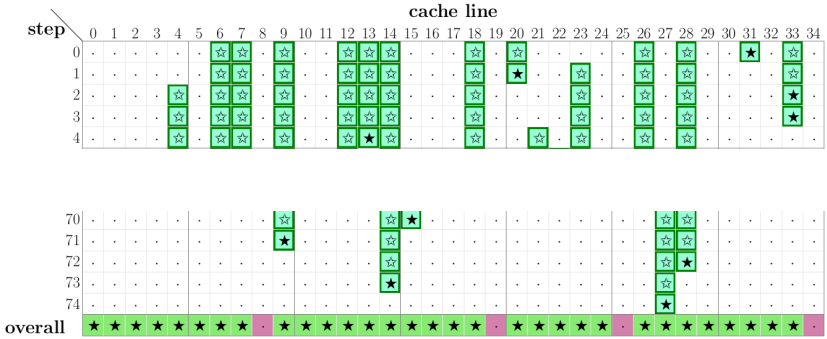

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- See paper for more details
  https://eprint.iacr.org/2023/102.pdf