

Speculative Execution and Cache Attacks

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Cyber in Saint-Malo, France

Computer Revolution

Computer Revolution

Processor speed

Memory latency

1977



1 MHz

500 ns

Computer Revolution

Processor speed

Memory latency

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1 MHz

500 ns

2020



20×3700 MHz

50 ns

Bridging Speed Gap

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 - ▶ spatial: divide memory into **lines**

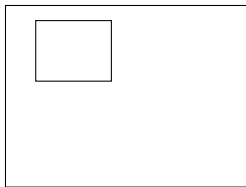
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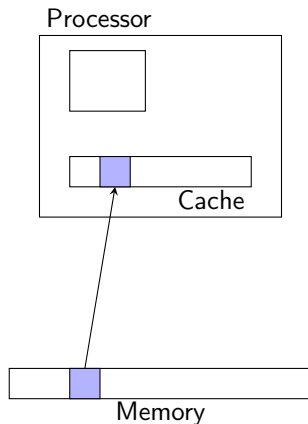
Processor



Memory

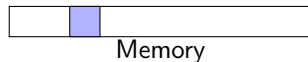
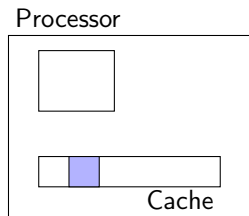
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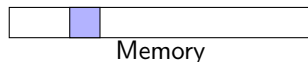
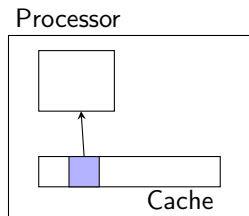
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 - ▶ spatial: divide memory into **lines**
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- Check if data is in cache



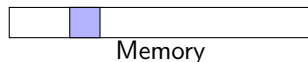
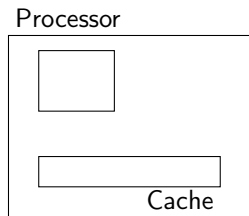
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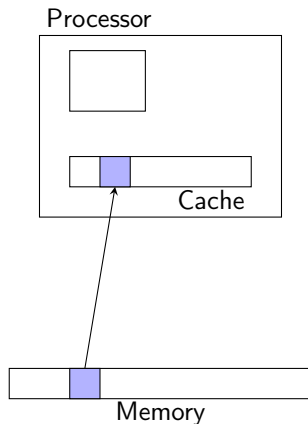
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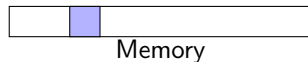
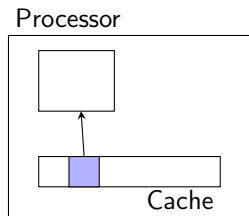
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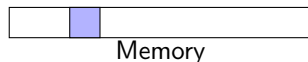
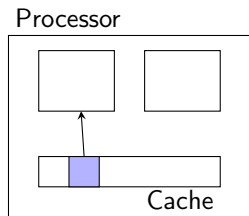
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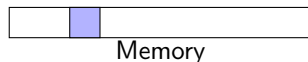
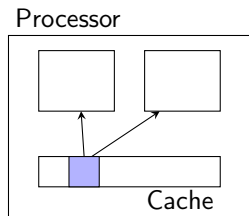
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- Share cache
 - ▶ improve performance of multi-core processors



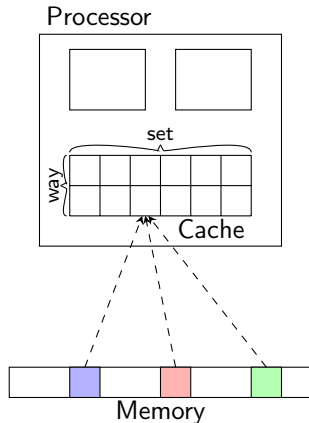
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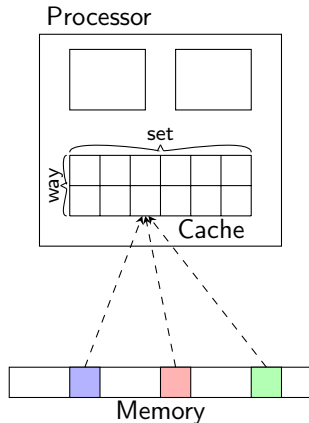
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- Memory lines map to **cache sets**



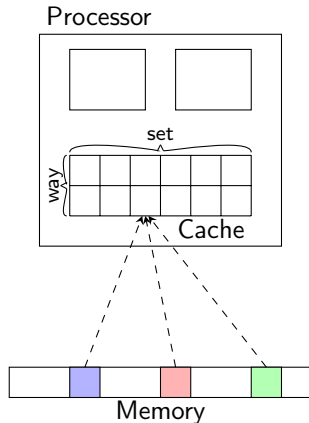
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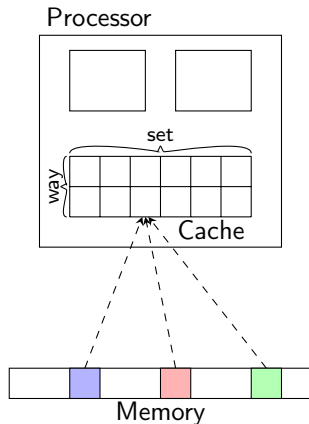
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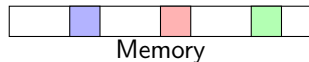
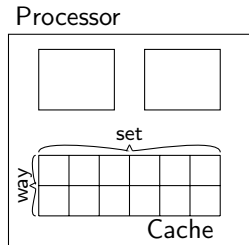
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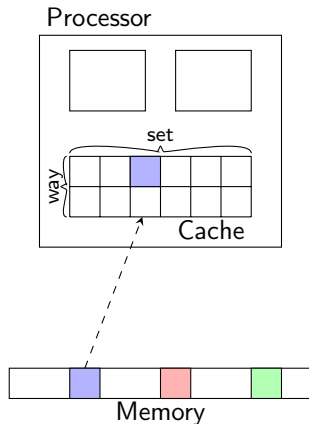
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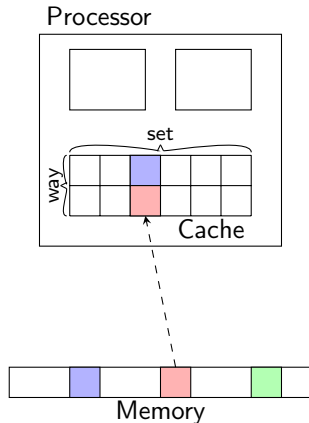
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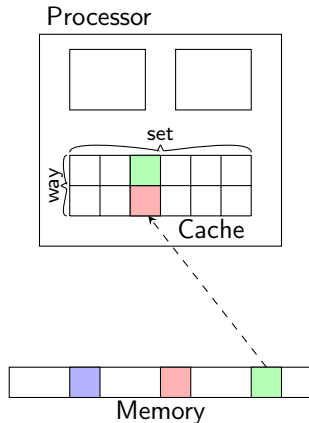
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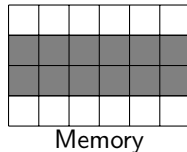
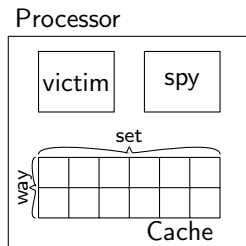
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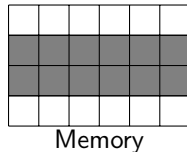
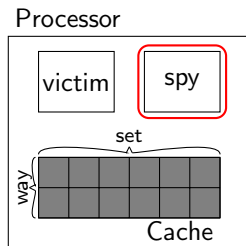
Prime + Probe [OST05, Per05]

- (Allocate cache-sized memory buffer)
- **Prime**: access all lines in buffer
→ fill cache with attacker's data
- Wait (victim executes)
→ may evict some cache lines
- **Probe**: measure time to access buffer
 - ▶ slow → cache line evicted
 - ▶ fast → no victim access



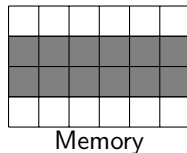
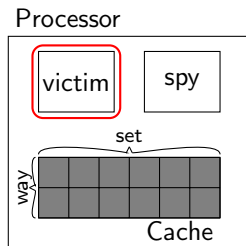
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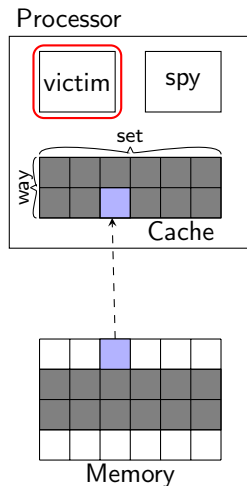
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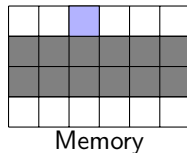
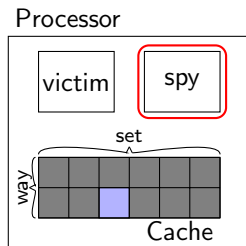
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- Accessing memory sets a state to **TRUE**
 - ▶ may also set another to **FALSE**
- Measuring access time observes state (and set to **TRUE**)

Conditional Access

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can execute even condition is FALSE

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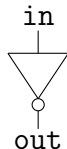
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`out = NOT(in)`



Other Functions

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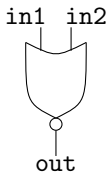
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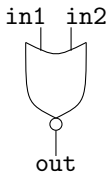
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out = NOR(in1,in2)
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if (*in1 + *in2 == 99)
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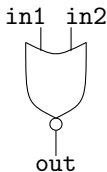


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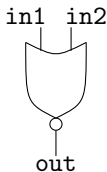
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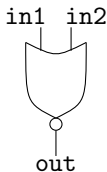
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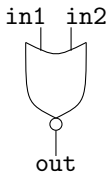
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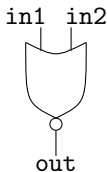
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if (*in1 == 99)
    return
if (*in2 == 99)
    return
a = *out
```

```
if (*in1 + *in2 == 99)
    return
a = *out
```

*in1	*in2	*out
FALSE	FALSE	TRUE
FALSE	TRUE	FALSE
TRUE	FALSE	FALSE
TRUE	TRUE	FALSE



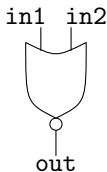
out = NOR(in1,in2)

*in1	*in2	*out
FALSE	FALSE	TRUE
FALSE	TRUE	TRUE
TRUE	FALSE	TRUE
TRUE	TRUE	FALSE

Other Functions

```
if (*in1 == 99)
    return
if (*in2 == 99)
    return
a = *out
```

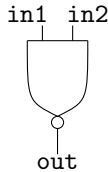
*in1	*in2	*out
FALSE	FALSE	TRUE
FALSE	TRUE	FALSE
TRUE	FALSE	FALSE
TRUE	TRUE	FALSE



out = NOR(in1,in2)

```
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    return
a = *out
```

*in1	*in2	*out
FALSE	FALSE	TRUE
FALSE	TRUE	TRUE
TRUE	FALSE	TRUE
TRUE	TRUE	FALSE



out = NAND(in1,in2)

Quiz Time

```
if (*in1 + *in2 == 99)
    return
if (*in2 + *in3 == 99)
    return
if (*in1 + *in3 == 99)
    return
a = *out
```

Quiz Time

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FALSE	FALSE	TRUE	TRUE
FALSE	TRUE	FALSE	TRUE
FALSE	TRUE	TRUE	FALSE
TRUE	FALSE	FALSE	TRUE
TRUE	FALSE	TRUE	FALSE
TRUE	TRUE	FALSE	FALSE
TRUE	TRUE	TRUE	FALSE

out = NOT(major(in1,in2,in3))

Multiple Outputs

Multiple Outputs

- Needed because gates destroy their inputs

Multiple Outputs

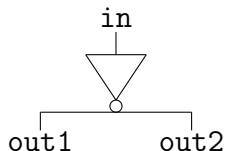
- Needed because gates destroy their inputs

```
if (*in == 99)
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a = *out1 + *out2
```

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- Needed because gates destroy their inputs

```
if (*in == 99)
    return
a = *out1 + *out2
```



Circuits

Circuits

- 4-bit ALU
 - ▶ 1 258 gates, 84-95% accuracy

Circuits

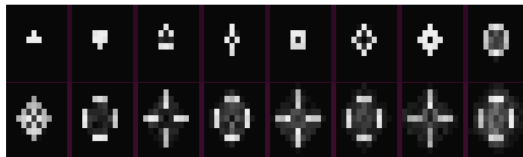
- 4-bit ALU
 - ▶ 1 258 gates, 84-95% accuracy
- SHA-1
 - ▶ one round: 2 208 gates, 95% accuracy

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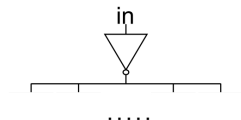


Amplification

- NOT gate with large fan-out

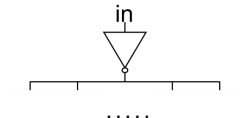
Amplification

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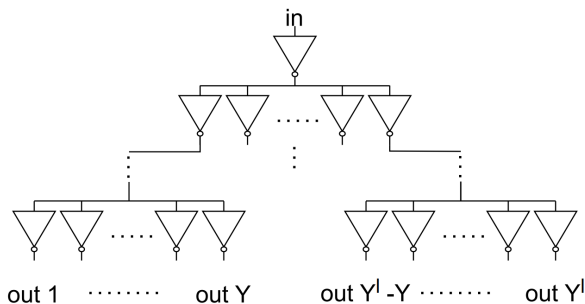
```
if (*in == 99)
    return
```

```
a = *out1 + *out2 + *out3 + *out4 + *out5 + *out6 + *out7 + *out8
```

Amplification

- NOT gate with large fan-out (e.g., $Y = 8$)

- ▶ $l = 2$ layers: 64
- ▶ $l = 3$ layers: 512
- ▶ $l = 4$ layers: 4 096



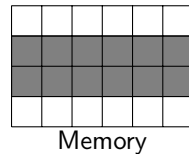
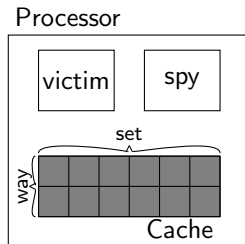
```
if (*in == 99)
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```

Prime+Store: High-Resolution Prime+Probe

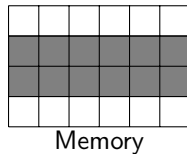
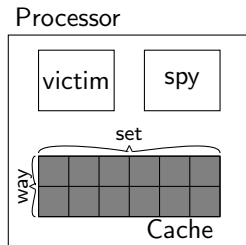
Prime+Store: High-Resolution Prime+Probe

- Prime as in Prime+Probe



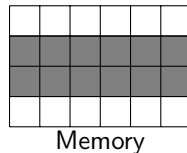
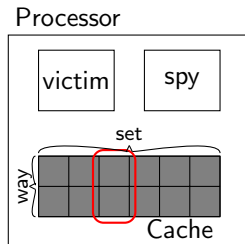
Prime+Store: High-Resolution Prime+Probe

- Prime as in Prime+Probe
- Probe is basically a NAND gate



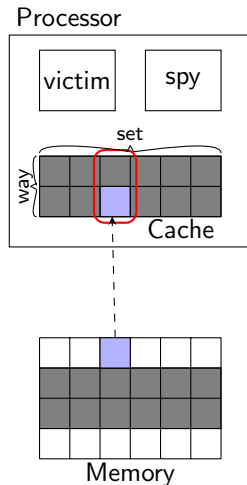
Prime+Store: High-Resolution Prime+Probe

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 - ▶ **FALSE** if all are cached



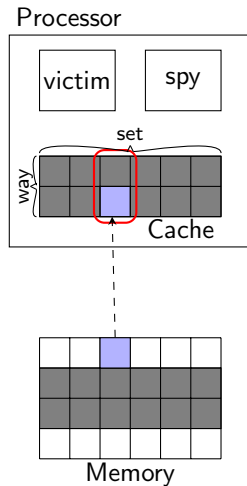
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Prime+Store: High-Resolution Prime+Probe

- Prime as in Prime+Probe
- Probe is basically a NAND gate
 - ▶ **FALSE** if all are cached
 - ▶ **TRUE** if some are not cached
- Do multiple probes of the same cache set and store results.



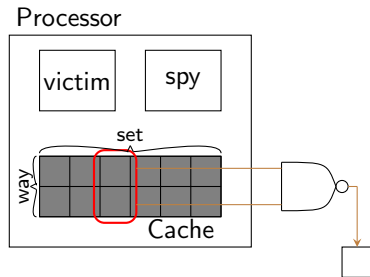
Prime+Store: High-Resolution Prime+Probe (cont.)

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- Decouple probe from time measurement

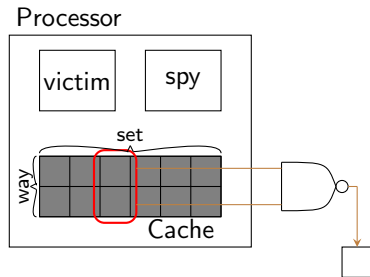
Prime+Store: High-Resolution Prime+Probe (cont.)

- Decouple probe from time measurement



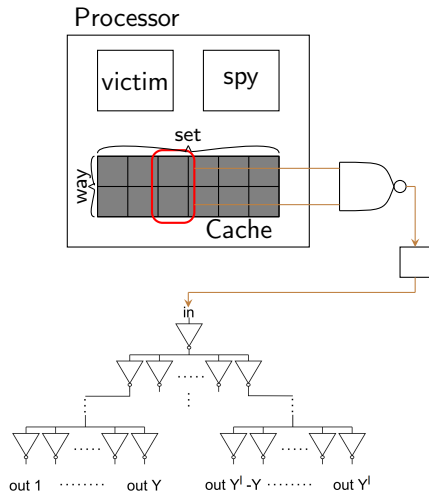
Prime+Store: High-Resolution Prime+Probe (cont.)

- Decouple probe from time measurement
- Measure time with amplification tree



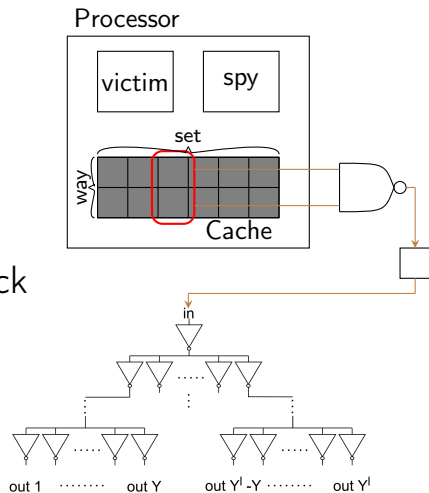
Prime+Store: High-Resolution Prime+Probe (cont.)

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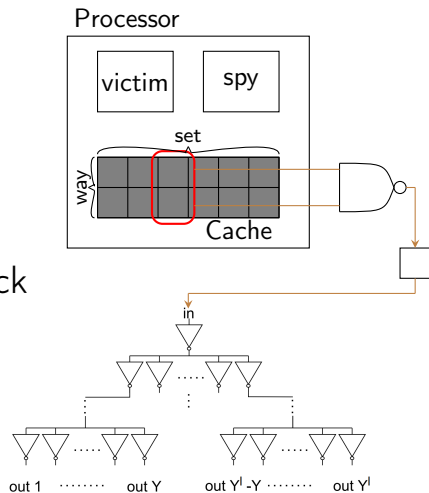
Prime+Store: High-Resolution Prime+Probe (cont.)

- Decouple probe from time measurement
- Measure time with amplification tree
- Attack square-and-multiply with slow clock



Prime+Store: High-Resolution Prime+Probe (cont.)

- Decouple probe from time measurement
- Measure time with amplification tree
- Attack square-and-multiply with slow clock
- Bypass countermeasure of reducing timer resolution



Challenges in Finding Eviction Sets

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- Cache replacement policies

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 - ▶ e.g., use physical addresses to map to cache sets of LLC
- Cache slicing
 - ▶ LLC is partitioned into many slices
 - ▶ The slice is determined by undocumented function

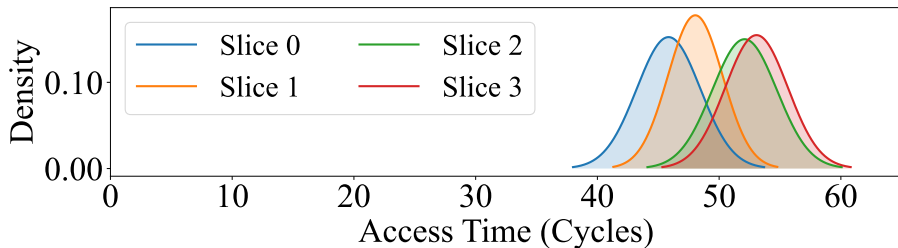
Slice Access Latency

Slice Access Latency

- Different LLC slices have different access time

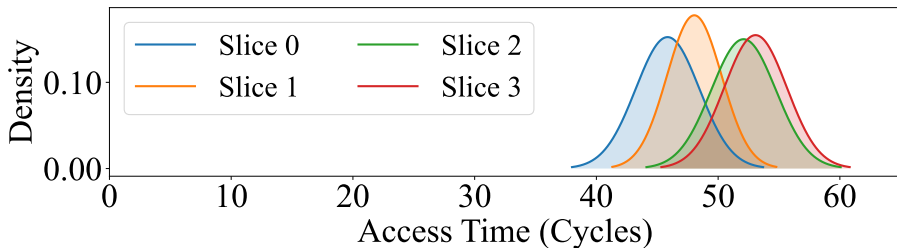
Slice Access Latency

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Slice Access Latency

- Different LLC slices have different access time
- Can we determine the slice index by the access time?



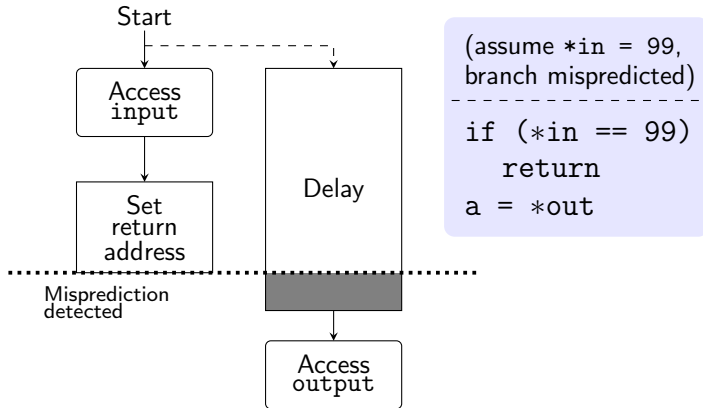
Weird Gate Operation

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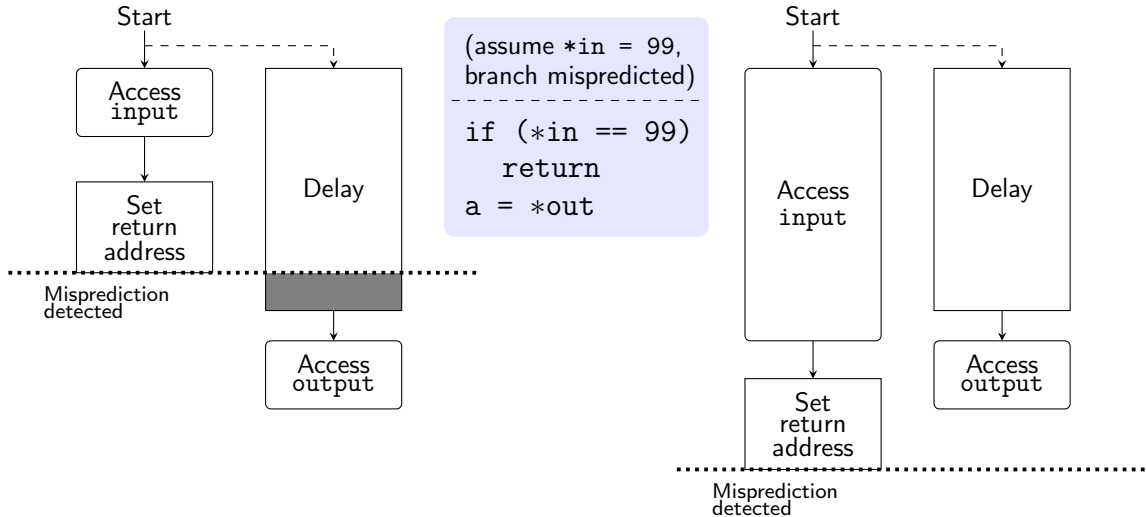
```
(assume *in = 99,  
branch mispredicted)
```

```
-----  
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    return  
a = *out
```

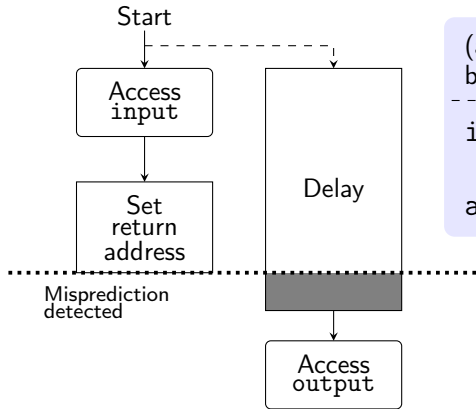
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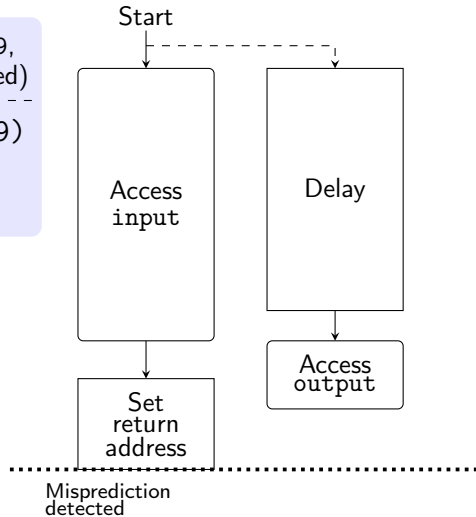
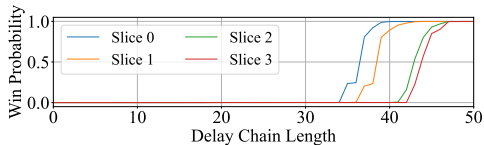
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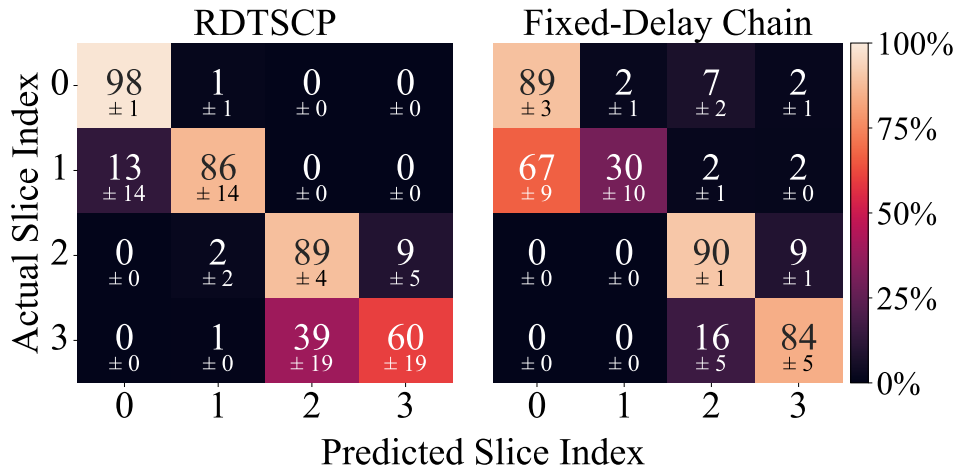
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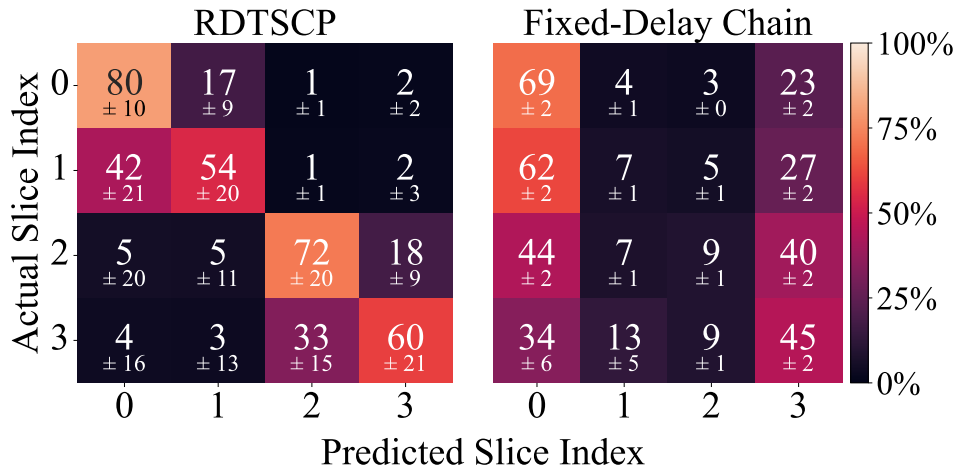
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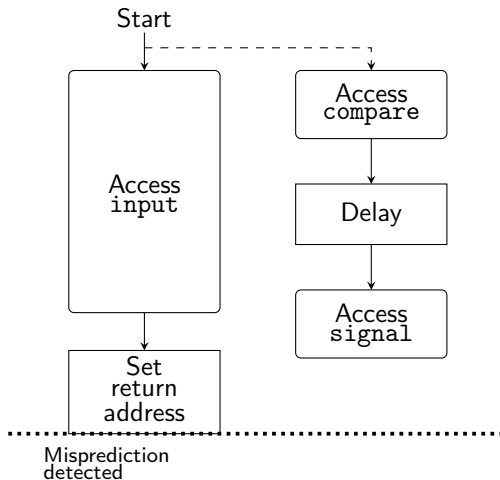
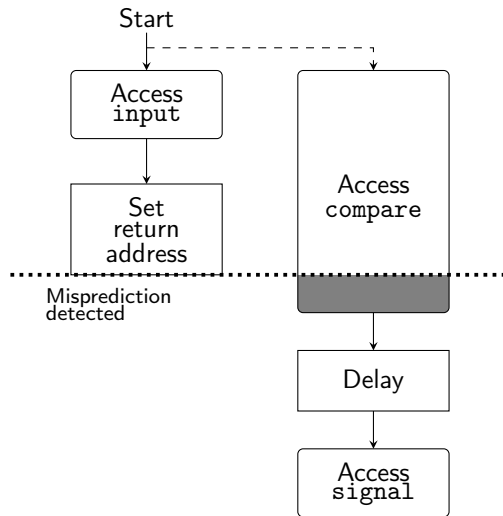
Slice Classification: quiet system



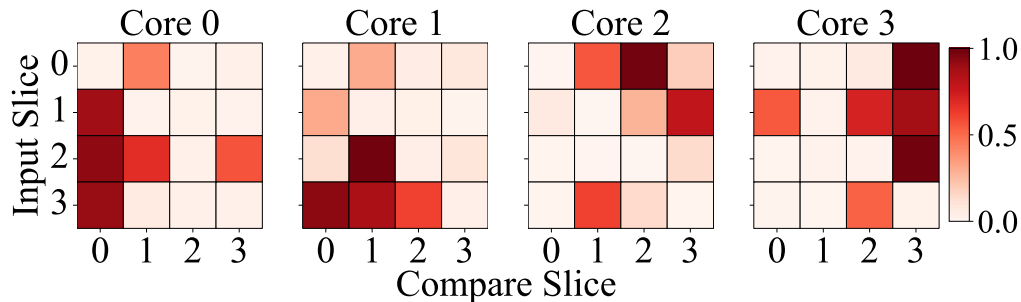
Slice Classification: busy system



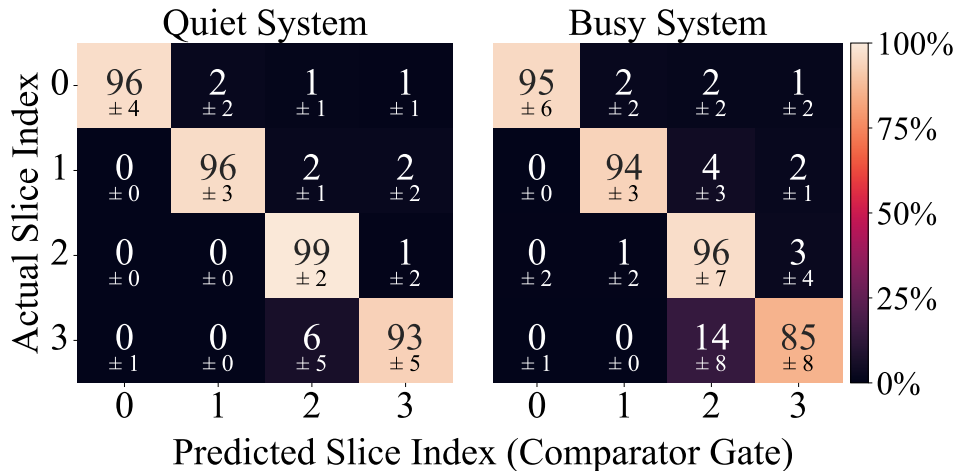
Comparator Gate



Comparator Gate: signal access



Slice Classification with Comparator Gate



Summary

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- Conditional speculative execution allows constructing logic gates

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- Cache-state logic gates are Turing-complete

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- Cache-state logic gates are Turing-complete
- Nested large fan-out gates amplify cache access signal
- Amplification enables detection with a slow clock
- Prime+Store decouples sampling from clock
- Comparator gate allows more accurate slice index determination