Evict+Spec+Time:Exploiting Out-of-Order Execution to Improve Cache-Timing Attacks

Chitchanok Chuengsatiansup

Joint work with Shing Hing William Cheng, Daniel Genkin, Dallas McNeil, Toby Murray, Yuval Yarom, and Zhiyuan Zhang

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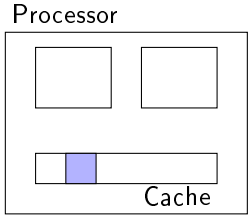

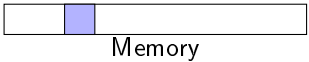

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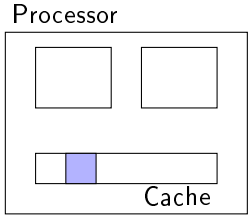

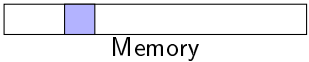

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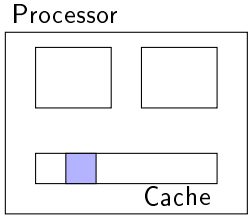

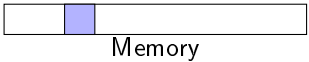

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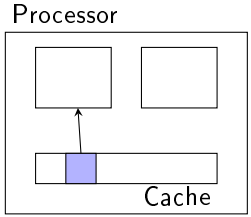

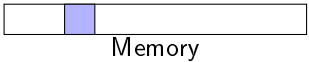

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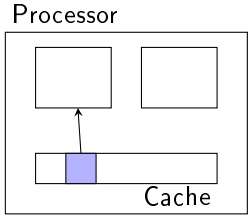

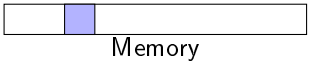

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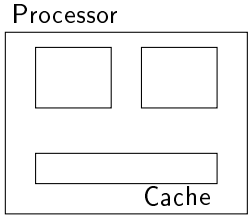

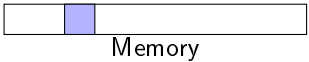

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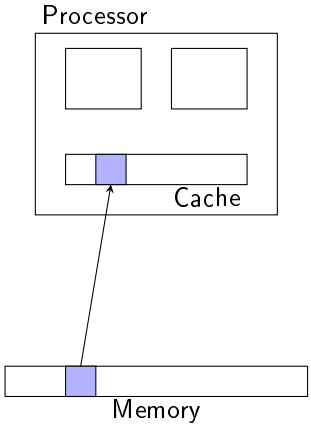

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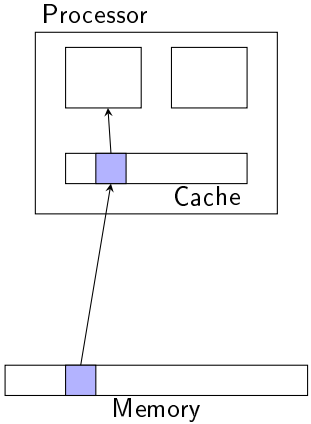

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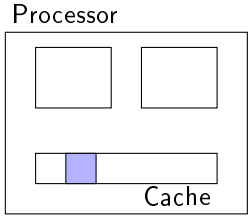

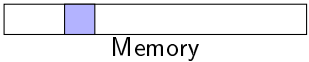

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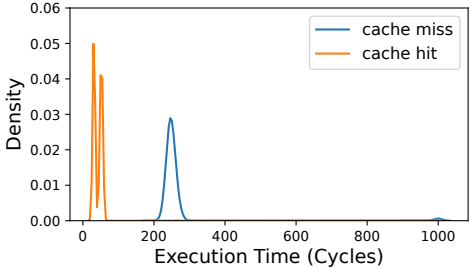

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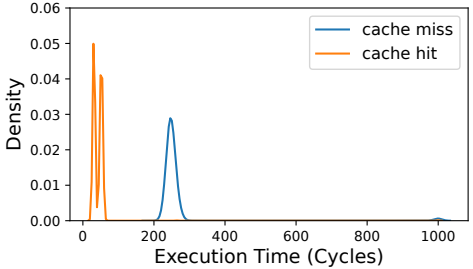

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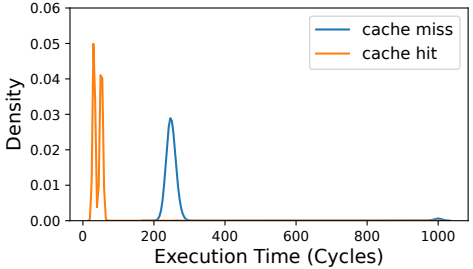

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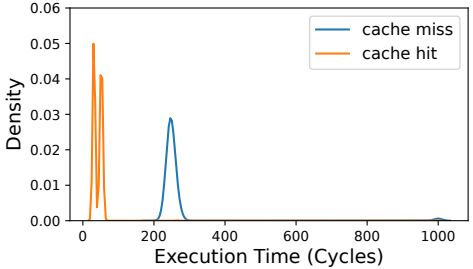

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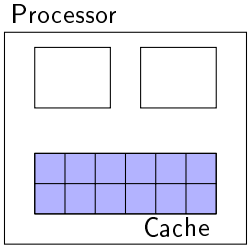

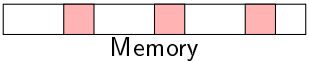

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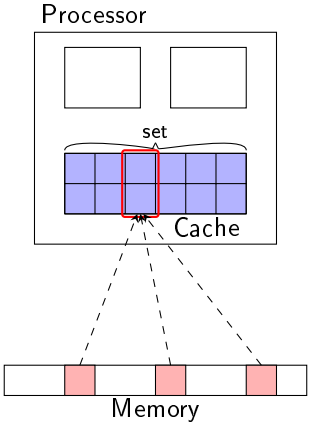

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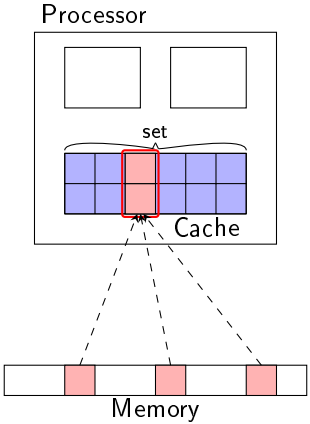

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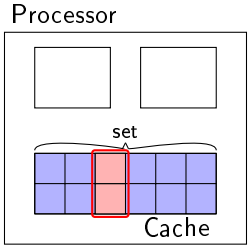

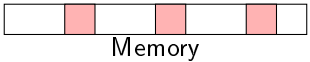

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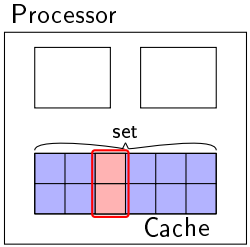

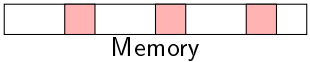

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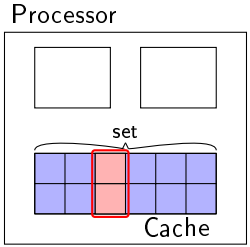

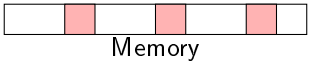

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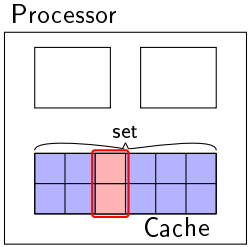

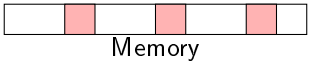

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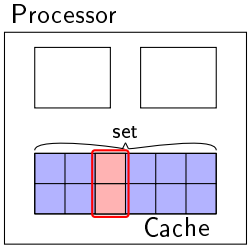

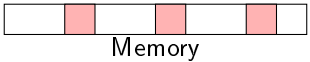

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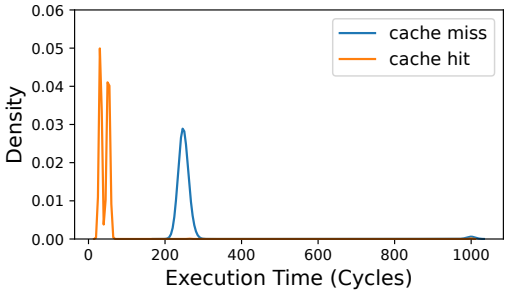

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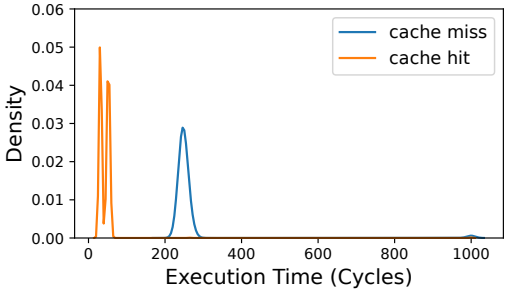

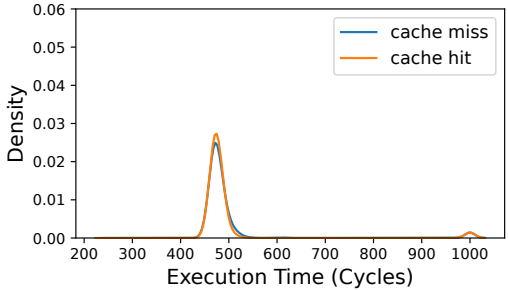

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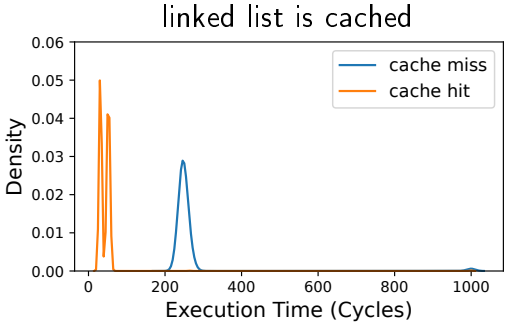

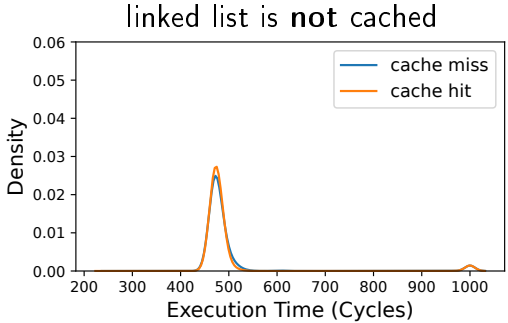

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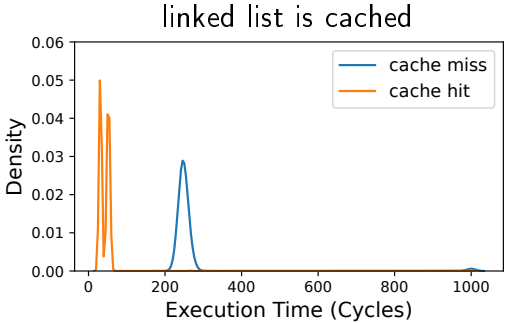

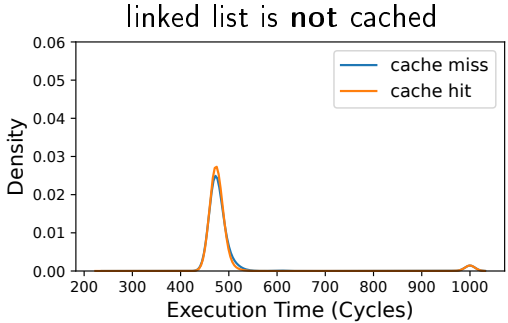

Latency is **not** additive because processors are superscalar

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How latency interacts with out-of-order execution?

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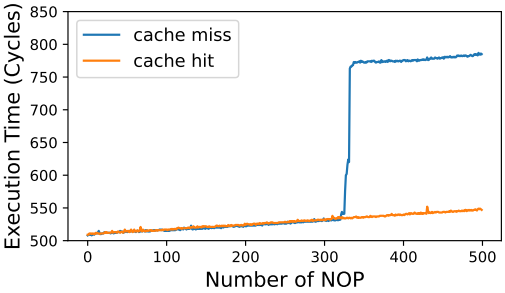

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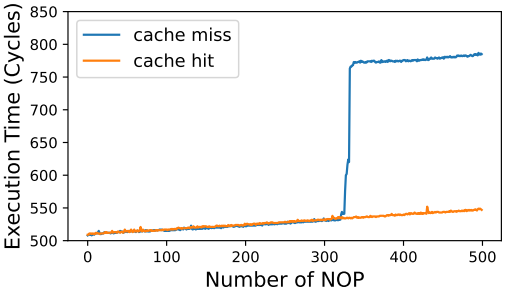

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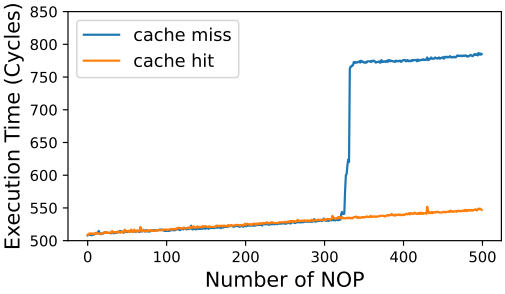


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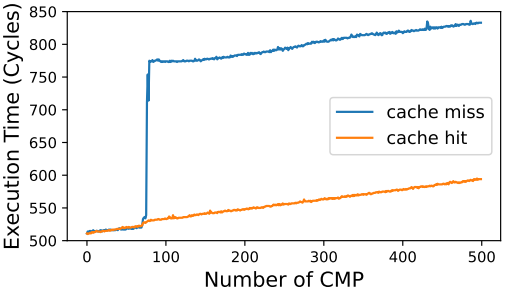

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  - depend on execution-time overlap
- Control resources can manipulate cache-miss latency hiding
  - allow us to identify when cache miss occurs
  - Evict+Spec+Time: know *when* beyond whether access occurs

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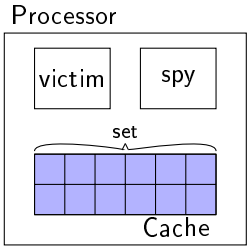

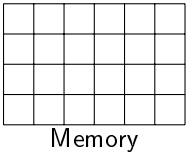

Evict+Spec+Time

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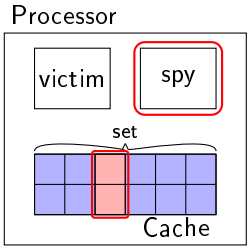

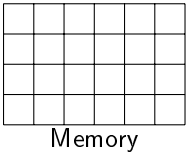

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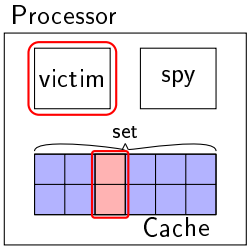

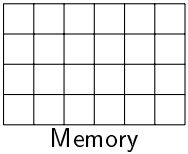

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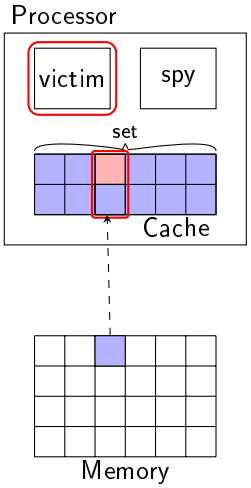

AES Decryption

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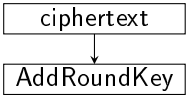

plaintext

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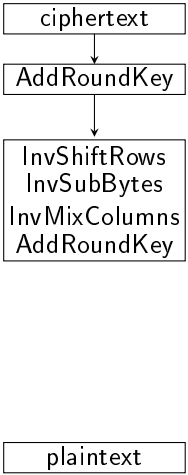

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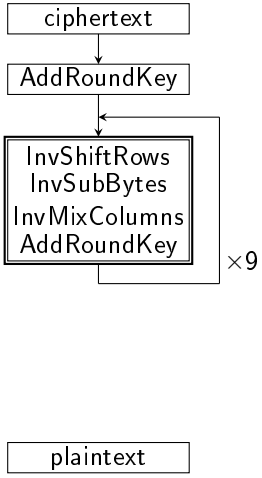

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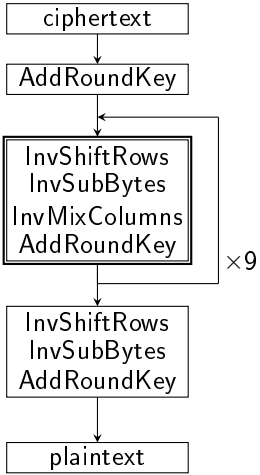

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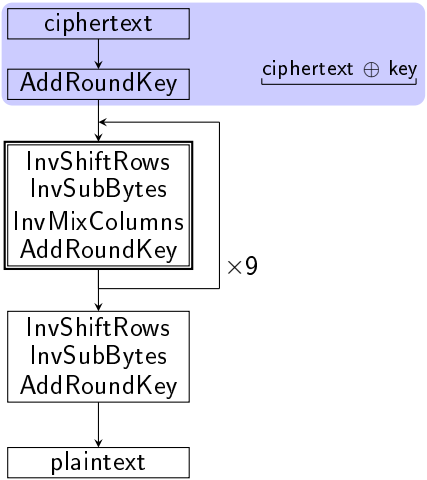

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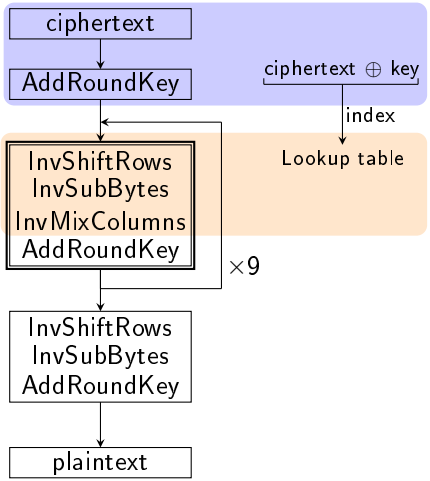

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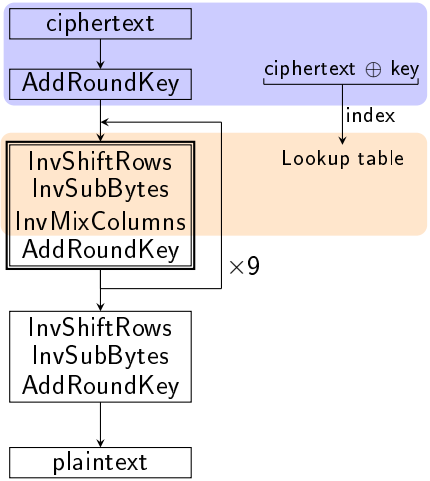

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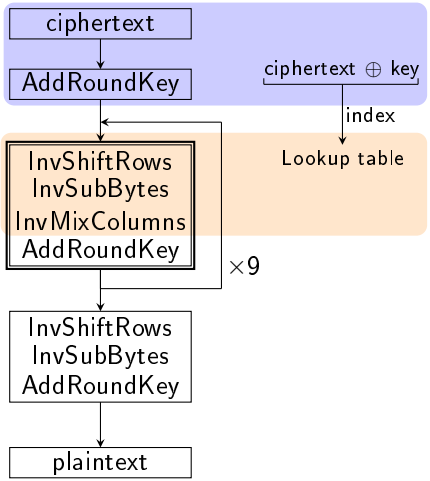

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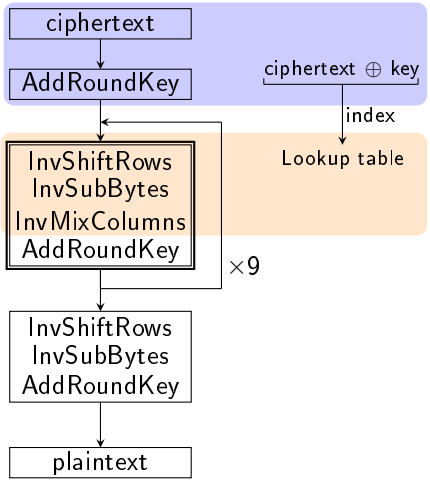

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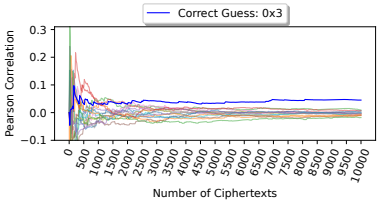

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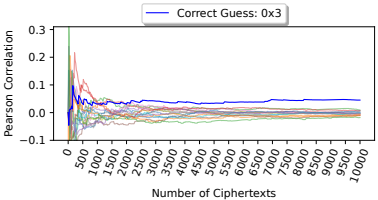

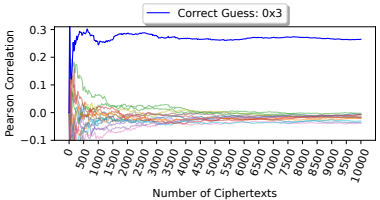

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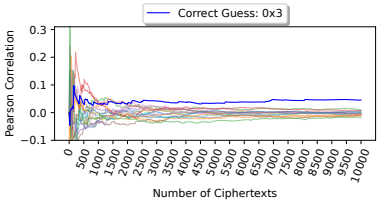

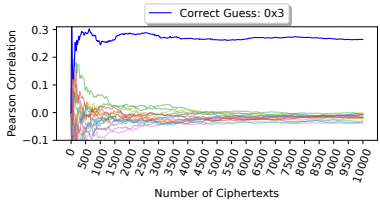

$\sim$ ten time higher prob. $\rightarrow$ $\sim$ ten time fewer samples

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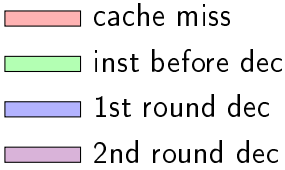

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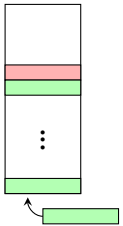

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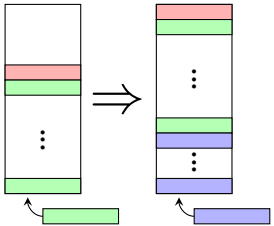

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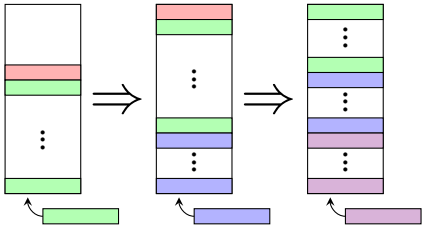

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- See paper for more details
  - https://eprint.iacr.org/2024/149.pdf